REMARKS / DISCUSSION OF ISSUES

Claims 5-20 are pending in the application.

The Office action rejects claims 5-13 and 16-19 under 35 U.S.C. 102(e) over Reiner (USP 5,995,629). The applicant respectfully traverses this rejection.

MPEP 2131 states:

> "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The ***identical invention*** must be shown in as ***complete detail*** as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 5, upon which claims 6-9 depend, claims a method that includes receiving input data into a second register at a first time, transferring the input data from the second register to a first register at a second time, performing functional operations on the input data in the first register to produce output data, transferring the output data to the first register, transferring the output data from the first register to the second register at a third time, and transferring the output data from the second register to an other component at a fourth time, wherein the segregation of the second and third times from the first and fourth times serves to mask data transfer operations.

The applicant respectfully maintains that Reiner does not teach transferring input data from a second register to a first register, does not teach transferring output data from a first register to a second register, and does not teach performing such transfers independent of transfers to and from an external component

Reiner fails to teach receiving input data into a second register at a first time, transferring the input data from the second register to a first register at a second time, and performing functional operations on the input data in the first register. Reiner's input data E is directly combined with output from Reiner's feedback unit RK, and the combination is placed directly into the shift register SR in the encoding unit VE.

Reiner fails to teach transferring output data from a first register to a second register and from the second register to an external component. The applicant claims placing the output data in a first register and then transferring the output data from the first register to the second register. The claims are amended to specifically recite that the same data ("the output data") that is placed in the first register is transferred from the first register to the second register. That is, upon transfer, the second register will contain the same information ("the output data") as the first register ("the output data").

The applicant respectfully maintains that Reiner's shift register AR does not contain the same information as the shift register SR. As taught by Reiner, and as illustrated in Reiner's FIG. 3, "the shift register SR generates a continuous sequence of data bits, although only some are fed to the output of the encoding unit VE as output data A, depending on the extraction unit AK" (Reiner, column 3, lines 44-47). Further, Reiner teaches that the extraction unit AK "combines certain states of the shift register SR non-linearly" to control which bits from the shift register SR form the output data A (Reiner, column 3, lines 34-40). That is, the shift register SR does not contain the output data A, per se; but rather, the shift register SR is a working register from which the output data A is generated as it receives input data E. Reiner's shift register AR contains Reiner's output data A, but, by specific and explicit design, this data is different from the contents of Reiner's shift register SR, because Reiner's shift register SR is configured to non-linearly generate the output data A, rather than to contain this output data A.

Because Reiner does not teach transferring input data from a second register to a first register, and does not teach transferring output data from a first register to a second register, and because Reiner does not teach performing such transfers independent of transfers to and from an external component, as specifically claimed in claim 5, the applicant respectfully maintains that claims 5-9 are patentable under 35 U.S.C. 102(b) over Reiner, per MPEP 2132.

Claim 10, upon which claims 11-16 depend, claims an integrated circuit that includes a processor that performs a given set of functional operations to execute an intended algorithm, based on input data in the first data register, and transfers output data to the first data register, and a controller that transfers the input data from a second data register to the first data register and the output data from the first data register to the second data register according to a first time sequence, and transfers the input data from the other component to the second register and the output data from the second register to the other component according to a second time sequence, the second time sequence being substantially uncorrelated with the first time sequence.

The applicant respectfully maintains that Reiner does not teach transferring input data from a second data register to a first data register, does not teach a processor that transfers output data to the first register, and a controller that transfers this output data from the first data register to the second data register, and does not teach transferring the input and output data to and from the second data register independent of the transfers to and from the first data register.

Reiner teaches that the input data E is combined with feedback data RK and loaded directly into shift register SR for operations by the encoding unit VE. Thus, Reiner cannot be said to teach a controller that transfers the input data from a second data register to the first data register.

Reiner teaches that the shift register SR is used to generate output data using a non-linear switching sequence. Thus, Reiner cannot be said to teach a processor that transfers output data to a first register and a controller that transfers this same output data to a second register.

Because Reiner does not teach the claimed transfers to and from the first register, Reiner cannot be said to teach transfers to and from an external component that are independent of these (non-existent) transfers to and from the first register.

Because Reiner does not teach a controller that transfers input data from a second data register to a first data register, and does not teach a processor that transfers output data to the first register, and does not teach a controller that

transfers this output data from the first data register to the second data register, and does not teach transferring the input and output data to and from the second data register independent of the transfers to and from the first data register, the applicant respectfully maintains that claims 10-13 and 16 are patentable under 35 U.S.C. 102(b) over Reiner, per MPEP 2132.

Claim 17, upon which claims 18-20 depend, claims an apparatus that includes a controller that controls transfer of a set of input data from a second register to a first register so that a processor can perform a sequence of functional operations related to the set of input data at the first register to produce a set of output data, and controls transfer of the set of output data from the first register to the second register.

As noted above, Reiner does not teach transferring input data from a second register to a first register, and does not teach transferring output data from the first register to the second register. Thus, Reiner cannot be said to teach a controller that performs these data transfer operations.

Because Reiner does not teach a controller that controls transfer of a set of input data from a second register to a first register so that a processor can perform a sequence of functional operations related to the set of input data at the first register to produce a set of output data, and controls transfer of the set of output data from the first register to the second register, the applicant respectfully maintains that claims 17-19 are patentable under 35 U.S.C. 102(b) over Reiner, per MPEP 2132.

The Office action rejects claims 14, 15, and 20 under 35 U.S.C. 103(a) over Reiner. The applicant respectfully traverses these rejections.

MPEP 2142 states:

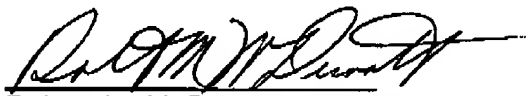
> "To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***... If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Claims 14 and 15 are dependent upon claim 10, and claim 20 is dependent upon claim 17. In support of this rejection, the Office action relies on Reiner for teaching the elements of claims 10 and 17 (Office action, page 5, first sentence of paragraph 13).

As noted above, Reiner fails to teach the elements of claims 10 and 17, and therefore the applicant respectfully maintains that the rejection of claims 14, 15, and 20 under 35 U.S.C. 103(a) over Reiner is unfounded, per MPEP 2142.

In view of the foregoing, the applicant respectfully requests that the Examiner withdraw the rejections of record, allow all the pending claims, and find the application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Robert M. McDermott, Attorney
Registration Number 41,508
patents@lawyer.com

1824 Federal Farm Road
Montross, VA 22520
Phone: 804-493-0707
Fax: 215-243-7525